

FIG. 1

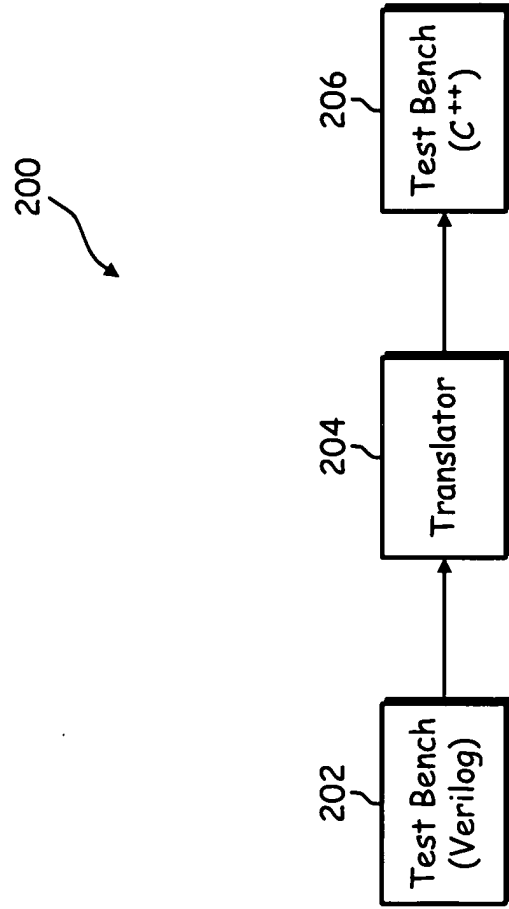


FIG. 2

VERILOG PATTERN	C++ PATTERN / ACTION
# Delay Statements	Remove # Delay Statements
' `ifdef Statements	Translate `ifdef Statements
' Symbols	Remove ' Symbols
Begin	{
End	}
Register Definitions	Convert Register Definitions
Combinatorial Assignments	Convert Combinatorial Assignments
Events	Convert Events
Verilog Switches	Convert Verilog Switches
Verilog Concat Expressions	Convert Verilog Concat Expressions
Verilog Parameters	Convert to C++ #Defines
Verilog Consts	Convert to C Consts
Verilog Bit Access Macro	Convert Bit Access Macro

FIG. 3

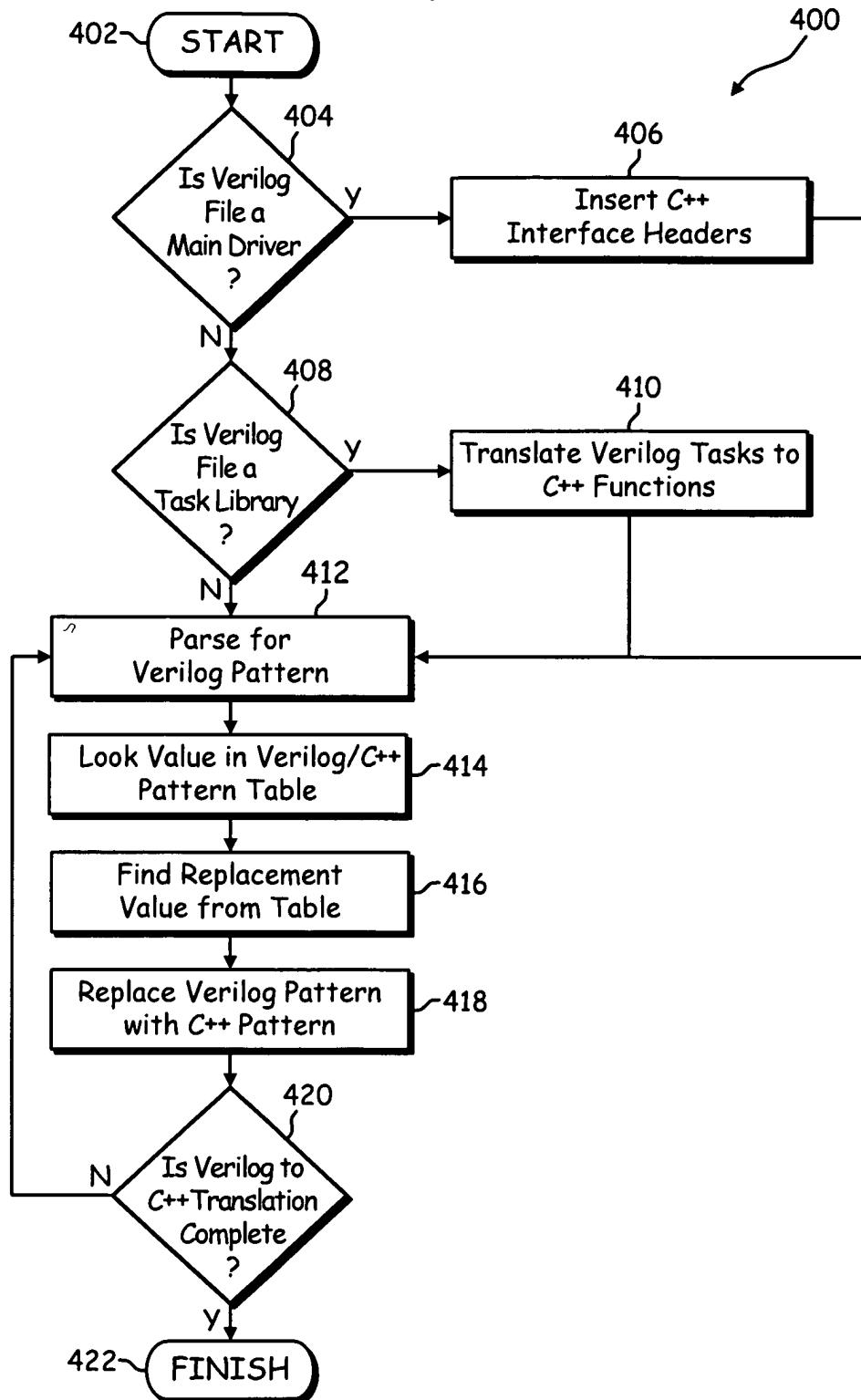


FIG. 4

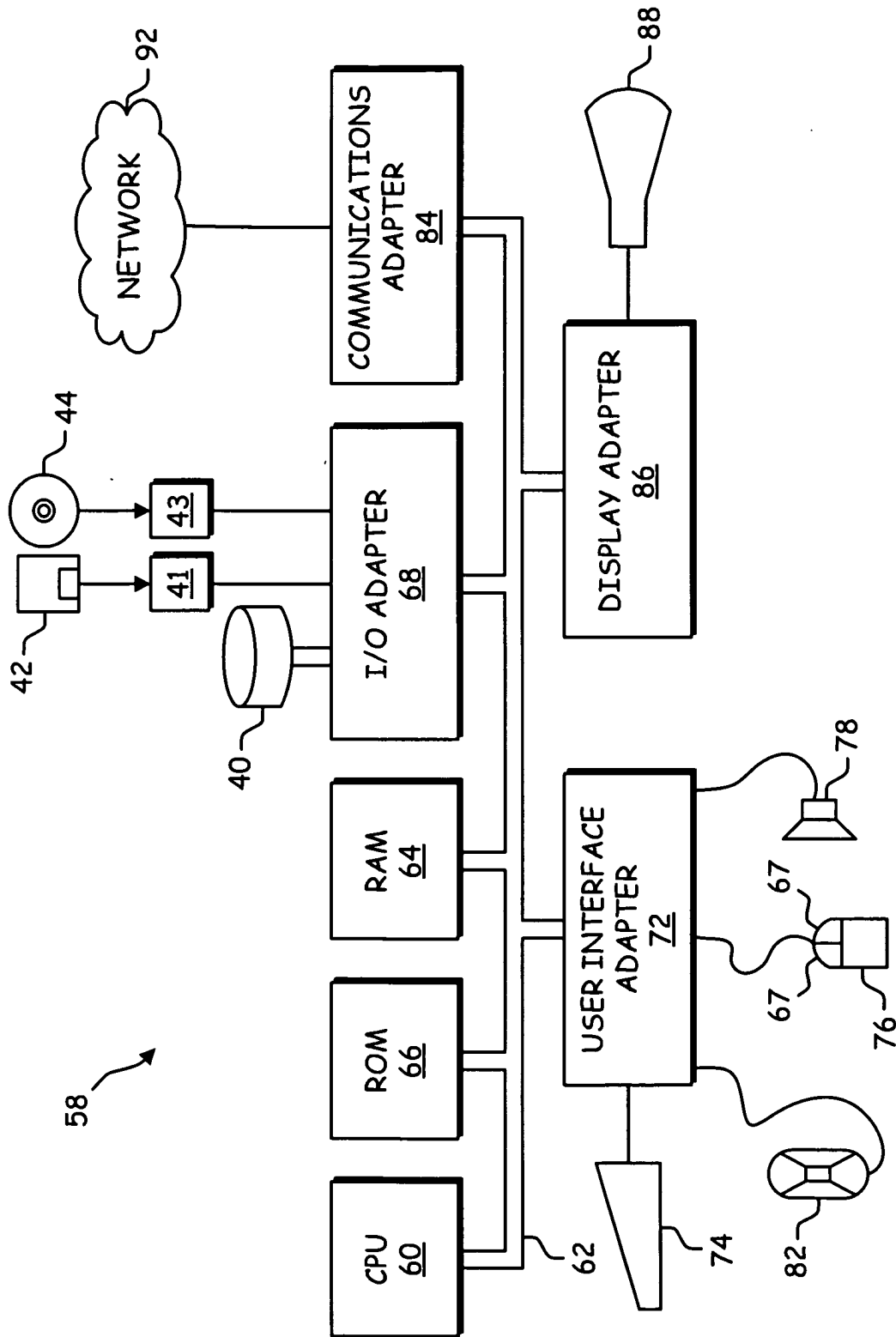


FIG. 5